Room Temperature Single-Electron Transistor Featruing Gate-Enhanced ON-State Current

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Abstract—A single-electron transistor operating at room temperature was successfully fabricated by an improved nanodamascene process. It consists in a gated titanium nanowire interspersed by two very closely spaced tunnel junctions constituting a Coulomb Island. The improvement in the process concerns the presence of an individual control gate close to the island, paving the way toward the fabrication of single-electron circuits. Moreover, a final oxidizing plasma treatment was used to tune the tunnel junction capacitances and, thus, the device operating temperature. As expected, electrical characteristics showed Coulomb blockade at room temperature, with an unexpectedly high ON-state current.

Index Terms—Nanodevice, nanotechnology, plasma oxidation, room temperature, single-electron transistor (SET).

I. INTRODUCTION

SINGLE-ELECTRON devices (SEDs) have attracted much attention since the 1980s when it has become clear that they could be used to fabricate low-power logic devices, high-performance sensors, and metrological standards [1], [2]. Among SEDs, single-electron transistors (SETs) have been the most studied devices because they were seen as a potential successor for present metal–oxide–semiconductor (MOS) transistors. However, SETs are known to face important drawbacks: in most cases, they work at cryogenic temperature, deliver low ON-state currents, and are fabricated with processes that are poorly compatible with complementary-MOS (CMOS) standards, although emerging devices are required to feature CMOS compatibility in order to favor hybrid circuit fabrication [3]. Recently, a “nanodamascene process” has been proposed to elaborate titanium islands weakly coupled to titanium nanowires [4]. This resulted in double tunnel junctions (DTJs) using the underlying substrate as a back-gate to exhibit CB oscillations at room temperature with ON-state currents of a few tens of nanoamperes. Moreover, the nanodamascene process offers promising prospects in terms of CMOS compatibility. Indeed, although it involves e-beam lithography steps, the spatial resolution required for room temperature operation is within reach of current photolithography technologies. In the same way, the liftoff step could be replaced by a blanket metal deposition followed by a dry etch selective to the silicon oxide. However, the use of global back-gates implies that many DTJs present on a chip cannot be addressed individually, while the fabrication of circuits requires independently gated devices. The purpose of this letter was therefore to fabricate selectively tunable SETs with the nanodamascene process. This was a challenge for two reasons. First, a finely controlled alignment step is required for positioning the island at the chosen distance from the control gate. Second, in general, the presence of a gate is expected to increase the total capacitance of the island, decreasing, in turn, the charging energy of the SET and then the operation temperature. Thus, it is of high interest to be able to decrease the other capacitances to keep the devices operating at room temperature. Within this framework, this letter shows that a fine control of the total capacitance can be achieved by O₂ plasma oxidations and immediate electrical characterizations until the CB is observed at room temperature. In addition, the drain-source current was found to increase with the gate bias more than expected, because of the modification of the barrier shapes by the gate electric field.

II. EXPERIMENT

The nanodamascene process is extensively described elsewhere [5]. It is briefly summarized here, with an emphasis on the modifications we brought to maintain room temperature operation with the presence of a local gate. The first step consisted in electron beam direct writing in a 100-nm-thick SiO₂ layer intending to form trenches after development. A first single-line trench was patterned with an energy of 2 keV and a dose of 600 nC/cm to constitute the drain and the source. A 100-nm-wide perpendicular gate was also patterned with an energy of 2 keV and a dose of 80 mC/cm², 75 nm away from the drain/source trench. The development step was achieved with a 6 : 1 : 43 NH₃F : HF : H₂O solution, etching the irradiated area three times faster than the rest of the oxide. A 40-nm-wide and 25-nm-thick titanium line perpendicular to the drain/source trench was then created by liftoff to be finely aligned to the gate trench. As shown by Fig. 1(a), this was achieved with an accuracy of about 10 nm. This line will constitute the island at the end of the process. The tunnel junctions were formed by oxidation at room temperature of the island line in a pure O₂ plasma carried out in a PLASMALINE 211 barrel ashier at 50 W for 2 min. Next, a 25-nm-thick titanium “blanket” layer was deposited over the entire sample and Chemical-Mechanical Planarization (CMP) was performed to remove this blanket at the surface of the sample while keeping the material deposited in the trenches. The CMP step was achieved on an ULTRATEC Multipol CMP system, using a 0.05-μm colloidal silica slurry, with a pressure of 280 g/cm² and a rotation speed of 15 r/min. Electrical contacts were finally patterned by an electron beam...
This case, we restricted the gold electrodes do not oxidize during plasma steps, and in Fig. 2. The electrical characterization is possible because the characteristics after each oxidation, as shown by the inset of $I_D-V_{DS}$ plot of the SET at 300 K after the complete plasma oxidation (8 min). Data are represented by points and solid lines are SIMON simulations (see Fig. 3 for parameters). Inset: $I_D-V_{DS}$ plot of the SET at room temperature with the gate grounded, before oxidation (□) and during the oxidation process (◆ after 1 min, △: 3 min, and ◊: 8 min).

In Fig. 2, $I_D-V_{DS}$ plot shows a very clear nonlinear behavior: The current decreases when the voltage is swept, which is characteristic of an ohmic conduction mode with no noticeable CB. This behavior is typical of a SET measured above its operation temperature, which means that one has to decrease the total capacitance of the island. Successive oxidations give rise to a gradual decrease of current that cannot only be attributed to CB, but also to the increasing resistivity of the electrodes: indeed, they are oxidized from their surface, and their section therefore decreases during the oxidation. To check if the room temperature CB regime was reached, the drain–current measurement was carried out with a larger $V_{DS}$ range, from −1.2 to +1.2 V, with different gate bias values ranging from 0 to 2.5 V (Fig. 2). For $V_G = 0$ V, the $I_D-V_{DS}$ plot shows a very clear nonlinear behavior: The current is suppressed, with a threshold voltage of about ±0.45 V. As expected by CB “orthodox theory” [1], [2], the nonlinearity was gradually suppressed with increasing gate voltages and a gate bias ($V_G = 2.5$ V) was found to make the drain current linear with $V_{DS}$. This gate bias is well above the threshold voltage evidencing that the voltage gain is inferior to one. Gate biases superior to 2.5 V led to gate leakage current and breakdown, preventing the observation of $I_D-V_{DS}$ oscillations. In Fig. 2, $I_D-V_{DS}$ curves were fitted by using the software SIMON [6] with the resistance values plotted versus the gate bias and the capacitance parameters shown in Fig. 3. The total resistance is found to strongly decrease when the gate bias

![SEM picture of the active area of the SET](image1)

**III. RESULTS AND DISCUSSION**

In our process, the CMP step was stopped as soon as the blanket titanium layer was completely removed; only a very small Ti and SiO$_2$ thickness was therefore expected to be removed in the titanium nanowire and in the background oxide. As a consequence, the dimensions of the SET are quite large (~65 nm, see Fig. 1(a)), compared to what would be expected for a room temperature SET. Thin dark areas can be distinguished in the drain/source nanowire: these are the two tunnel junctions delimiting the 25-nm-wide island. The aim was to further reduce the Ti nanowire cross section with successive O$_2$ plasma oxidation steps in order to better control the decrease of the total capacitance, as well as the decrease of the conductivity of the device. Indeed, it is difficult to achieve further CMP steps once the characterization pads are processed. By contrast, it is very convenient to perform O$_2$ plasma steps and to observe the modifications on $I_D-V_{DS}$ characteristics after each oxidation, as shown by the inset of Fig. 2. The electrical characterization is possible because the gold electrodes do not oxidize during plasma steps, and in this case we restricted the $V_{DS}$ range to 0–0.5 V in order to limit the current flowing through the junctions. The linearity of the $I_D-V_{DS}$ curves is characteristic of an ohmic conduction
is increased a behavior that is not expected by CB “orthodox theory.” This suggests that, as shown in Fig. 4, the gate electric field thins and lowers the potential barriers, as it is commonly observed in metal/insulator tunnel transistors [7], [8]. It is worth noting that the ON-state current is high (tens of nanoamperes) when compared to the hundreds of femtoamperes driven by transistors reported to feature similar charging energy. Cases where $V_G = 0.5 \text{V}$ and $V_G = 1 \text{V}$ are also illustrated.

In conclusion, the nanodamascene process was improved to provide locally gated room temperature SET suitable for integration into circuits. The CMP step was stopped early, and the total capacitance of the device was finally decreased with a good control thanks to successive oxygen plasma oxidations and $I_D$–$V_{\text{DS}}$ measurements. Two features are important in this SET: first is its high current level, which considerably relaxes the tradeoff between conductivity and total capacitance, ensuring high-temperature and low-impedance operation. The second is the gate-induced potential barrier modification, which enables the SET to exhibit a high ON-state while still keeping low OFF-state thanks to CB. This opens the prospect of CMOS-compatible fabrication of nanometer-scale devices that overcome the OFF-state leakage issues encountered in ultrashort channel MOS transistors and the high-impedance issues commonly attributed to SETs. The nanodamascene process is currently being developed to provide an autoaligned gate closer to the island in the purpose to increase the voltage gain above unity.

### REFERENCES


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*Fig. 4. (a) Schematic band diagram of the conductive channel of the SET with no bias applied. “S” is the source, “I” is the island, and “D” is the drain. (b) Schematic band diagram of the source junction biased with such a voltage ($V_{\text{DS}} < 0.75 \text{V}$) that the barrier is in direct tunnelling mode at $V_G = 0 \text{V}$. Cases where $V_G = 0.5 \text{V}$ and $V_G = 1 \text{V}$ are also illustrated.*