SiO₂ shallow nanostructures ICP etching using ZEP electroresist

Marc Guilmain, Abdelatif Jaouad, Serge Ecoffey, Dominique Drouin *

Nanofabrication and Nanocharacterization Research Center, Université de Sherbrooke, Sherbrooke, Quebec J1K 2R1, Canada

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1. Introduction

Recently, a nanodamascene process was proposed to fabricate single electron transistors (SET) that could operate at high temperature [1]. This process uses electron beam lithography to pattern a trench in the oxide layer. The pattern is developed in buffered hydrofluoric acid (BHF) which etches exposed SiO₂ about three times faster than non-exposed oxide. Even though, the resulting trenches have a width and a depth of about 20 nm, exposing an organic resist and then transferring the pattern in the oxide by dry etching would provide a higher throughput (lower doses needed) and a better compatibility with a production environment.

Although SiO₂ dry etching is a well established process [2–4], there are very few processes that allow a nanometer scale depth control together with vertical sidewalls nanostructures. For such patterning, Maximov et al. [5] have used chromium as a hard mask, while nanoscale process using electroresists [6] have not been yet demonstrated for SiO₂. Even if a simple RIE systems could be used for nano pattern etching [7], the use of a supplemental ICP coil providing RF energy allow to initiate and to sustain a high density plasma even for low pressure and low power. This enables the control of the plasma energy and density independently from the platen power which provide the control on the ion bombardment. These independent controls give more flexibility on the process development and allow one to obtain high selectivity and mainly reduced LER. This parameter is critical in the fabrication of 10 nm width lines. The main challenge of such a nanometer scale process is related to the fact that current inductively coupled plasma (ICP) systems have special chamber geometries, RF source power, gas fluxes, chamber pressure, etc. which are designed and optimized for deep etching, high etch rates and high throughput. Moreover, to fabricate very high resolution patterns, very thin electroresists that have different properties from photoresists are needed, adding restrictions and challenges to recipe development.

We used ZEP520A as etching mask because it is a positive tone resist that has a resolution comparable to PMMA together with a higher sensitivity and a higher plasma etch resistance. The challenges in developing a plasma process to etch shallow trenches in thermal oxide were to obtain near vertical sidewalls and a line edge roughness (LER) of less than a nanometer. Significant improvements to the ZEP520A etch resistance and thus the resulting LER by lowering the platen temperature are presented. The effect of ICP system parameters such as chamber pressure, platen and coil power, on the etch profile and resist selectivity are also given.

2. Methodology

The samples used for the process development consist of (1 0 0) silicon substrate with 100 nm of thermally grown oxide diced in 1 cm × 1 cm pieces. The SiO₂ layer must be thicker than the 20 nm deep etching to isolate the devices (SET) from the substrate. The samples are first dehydrated in a stove for 30 min at 125 °C. ZEP520A diluted with a ratio of 2.4 in anisole is spun on the sample at 5000 rpm in order to have a thickness of about 90 nm. The resist is then baked on a hot plate at 180 °C for 5 min. Lines with a 150 nm pitch are patterned with an energy of 20 kV at doses ranging from 0.09 nC/cm to 0.15 nC/cm to obtain line widths between 15 and 30 nm. The development is done in O-xylene at room temperature for 75 s and MIBK is used to rinse the samples. Fig. 1 presents a cross section view of patterned 30 nm lines spaced by 150 nm in ZEP520A resist. It can be seen that the resist sidewalls are vertical. Finally, a post-bake at 125 °C for 30 min is done in a
stove as suggested in ZEP data sheet for wet etching. Czaplewski et al. [8] demonstrated that a heat treatment improves etch resistance and our experiment showed that this post-bake was helpful to reduce line edge roughness of etched lines. Fig. 2 compares the resulting etched lines with and without ZEP post-bake. The measurements were done by 3σ analysis using maximum derivative algorithm through the Spectel Research Measurement Software on about 400 nm length.

The system used in this study is a Multiplex Advanced Oxide Etch (AOE) ICP system from Surface Technology Systems (STS) with a 6 inches electrostatic chuck. The 1 cm² samples were fixed on 6 inches Si wafer using wax. As a starting point, we used CF₄ gas at 12 sccm with H₂ at 14 sccm and He at 140 sccm, the platen RF power was fixed at 50 W and the coil RF power at 100 W with a chamber pressure of 8 mT. Experiments were done by varying pressure and RF power on coil and platen individually to observe the effects of each parameter on sidewall angles, LER and selectivity.

We used scanning electron microscopy (SEM) to measure sidewall angle and SiO₂ etch depth. Measurements were done on several trenches cross-section on which the mean value was extracted. Ellipsometry was used to measure the ZEP thickness and deduce the etch rate.

3. Results

We first investigate the effect of the platen temperature on LER by varying it between 0 °C and –20 °C. Fig. 3a demonstrates that reducing the platen temperature reduce LER of etched lines. Indeed, a drastic decrease of LER is clearly observed at a –20 °C platen temperature as shown in Fig. 3b. To explain this, an analogy can be made with cold resist development which improves LER of ZEP after development [9] and the proposed hypothesis is as follow: the e-beam divides the resist’s chain molecule causing a variation of the molecular weight of the ZEP across the exposed line. Because the glass transition temperature depend on the molecular weight, cooling the sample cause the resist on the edge of the exposed line to freeze increasing its resistance to etching. A similar behavior was recently observed in an oxygen plasma to etch channels in PMMA [10] where the surface roughness at the bottom of the channels was temperature dependant.

To study the effect of the other parameters, a platen temperature of –20 °C was used. The chamber pressure and RF powers were varied once at a time, keeping the other parameters fixed. Figs. 4–7 present measured angle, LER and selectivity for each parameter.

As shown in Fig. 4b, pressure does not seem to have a strong impact on sidewalls angle as we measured only 1° variation for pressure between 4 mT and 10 mT. However, at 2 mT the angle decreased drastically. This behavior may be linked to the fact that a pressure strike of 12 mT is used in order to assist the ignition of the plasma and the desired pressure is stabilized only after 15 s which is around half the total etch time. LER also is not really affected by pressure as a variation of only 0.1 nm is measured when increasing pressure from 2 mT to 10 mT. Finally, the variation of the selectivity with pressure is as expected for deep SiO₂ etching [11,12]. In fact, pressure do not affect ZEP etch rate but a higher pressure increase SiO₂ etch rate as shown in Fig. 4a.
The effect of coil RF power is shown in Fig. 5 with the measured bias between platen and plasma ($V_{DC}$) in inset. The ion energy is related to $V_{DC}$, so increasing the coil power while keeping the platen power fixed increases the ion density at the expense of the ion energy [13]. Two regimes can be observed in Fig. 5: below 175 W, $V_{DC}$ is highly dependent to the coil power, but over 175 W, $V_{DC}$ is almost zero. In the first regime, LER seems to improve as the coil power increases (ion bombardment decreases) which show that the ZEP is less damaged. In the second regime, the contribution of physical etching is very small and thus, the system may be in a deposit-removal regime [14] which could explain the worsening of LER.

The effect of platen power is shown in Fig. 6. For low power, the sidewalls angle increase as the power increases because of the higher directionality of ions, but for high power the trend is inverted. This deterioration is probably due to the short etching time necessary to attain a 20 nm depth which is less than 20 s for platen power over 75 W. In these conditions, the transient regime is more important and while the plasma is not stable, the etching is unpredictable. As seen previously for coil RF power variation, more ion bombardment which is caused by an increase of bias power damages ZEP resist causing a higher LER. RIE cannot be used at low platen power because a minimum power is required to initiate the plasma. Increasing the RIE power to obtain a stable plasma will cause the LER to deteriorate as shown in Fig. 6.

Fig. 7 shows the effect of platen RF power with the coil fixed at 300 W. The sidewall angle presents a maximum which is similar to the trends seen when varying the platen power while keeping the coil fixed at 100 W. Power below 75 W is small compared to a 300 W on the coil, thus chemical etching is dominant and the plasma is less stable leading to variation of LER and selectivity.

Fig. 8 presents the resulting trenches in SiO$_2$ for this recipe when using a pressure of 8 mT, a coil power of 100 W and a platen power of 50 W. For the final recipe, the platen temperature should be maintained at a minimum to obtain the best LER. A pressure between 4 and 10 mT can be used because of its small impacts on results. A coil RF power between 100 W and 175 W gives good results but should not be increased furthermore. And finally, the sidewalls angle is maximal for a platen RF power of 50 W.

4. Conclusions

We demonstrated that ICP equipments which are designed for deep and fast etching can be used to etch shallow nanostructure with near vertical sidewall angle using a thin electroresist etch mask. A combination of a resist post-bake after development and a low platen temperature led to improved LER after etching.
Trenches of 20 nm wide and 20 nm deep with sidewalls angle of 86° and LER of less than 1 nm were achieved with the optimized stable and reproducible recipe.

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